AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) ~~The lead frame according to claim 1, further comprising:~~ A lead frame comprising:

a plurality of leads arranged in parallel, wherein

each of said leads is constituted by being divided into two portions of an inner lead portion and an outer lead portion,

said inner lead portion has a fine inner lead portion and a middle inner lead portion for interconnecting said fine inner lead portion and said outer lead portion,

said fine inner lead portion has a first thickness,

each of said middle inner lead portion and said outer lead portion has a second thickness and a second width,

said fine inner lead portion has a tip of a first width, and a rear stage expanded in width from the first width of said tip to the second width of said middle inner lead portion,

the first thickness is smaller than the second thickness, and

the first width is smaller than the second width; and

a plurality of spare leads each of which is constituted by being divided into two portions of a spare inner lead portion and a spare outer lead portion, wherein:

~~the~~ said spare leads are arranged in parallel to be apart from ~~the~~ said leads in areas between ~~the~~ said middle inner lead portions of the adjacent leads,; and

~~the~~ said spare leads are respectively arranged from a boundary between ~~the~~ said middle inner lead portion and ~~the~~ said fine inner lead portion of the adjacent lead to the area of ~~the~~ said outer lead portion side.

3. (Currently Amended) A semiconductor device~~, wherein~~ comprising:

a lead frame;

a first semiconductor element; and

a second semiconductor element, wherein:

said lead frame comprises a plurality of leads arranged in parallel;

each of said leads is constituted by being divided into two portions of an inner lead portion and an outer lead portion;

said inner lead portion has a fine inner lead portion and a middle inner lead portion for interconnecting said fine inner lead portion and said outer lead portion;

said fine inner lead portion has a first thickness;

each of said middle inner lead portion and said outer lead portion has a second thickness and a second width;

said fine inner lead portion has a tip of a first width, and a rear stage expanded in width from the first width of said tip to the second width of said middle inner lead portion;

the first thickness is smaller than the second thickness, and the first width is smaller than the second width;

an electrode of ~~a~~ said first semiconductor element is connected through flip chip bonding to ~~the~~ a respective one of said fine inner lead portions of ~~the~~ said lead frame ~~of claim 1~~ by a bump formed on the electrode;

~~a~~ said second semiconductor element is stuck to a surface opposite a surface of ~~the~~ said lead frame on which ~~the~~ said first semiconductor element is mounted by a semiconductor element adhesive;

one end of a wire is attached to an electrode disposed on a surface opposite the surface of ~~the~~ said second semiconductor element stuck to ~~the~~ said lead frame;

the other end of the wire is attached to ~~the~~ a respective one of said middle inner lead portions of ~~the~~ said lead frame;

resin sealing is executed to include ~~the~~ said inner lead portions of ~~the~~ said lead frame and ~~the~~ said first and second semiconductor elements; and

~~the~~ said outer lead portions of ~~the~~ said lead frame ~~is~~ are exposed from a resin-sealed portion.

4. (Currently Amended) A semiconductor device~~, wherein~~ comprising:

a lead frame;

two first semiconductor elements; and

two second semiconductor elements, wherein:

said lead frame comprises a plurality of leads arranged in parallel;

each of said leads is constituted by being divided into two portions of an inner lead portion and an outer lead portion;

said inner lead portion has a fine inner lead portion and a middle inner lead portion for interconnecting said fine inner lead portion and said outer lead portion;

said fine inner lead portion has a first thickness;

each of said middle inner lead portion and said outer lead portion has a second thickness and a second width;

said fine inner lead portion has a tip of a first width, and a rear stage expanded in width from the first width of said tip to the second width of said middle inner lead portion;

the first thickness is smaller than the second thickness, and the first width is smaller than the second width;

said two first semiconductor elements are connected through an anisotropic conductive sheet to front and back sides of ~~the~~ said fine inner lead portions of ~~the~~ said lead frame ~~of claim 1~~ by electrodes disposed on ~~the~~ said first semiconductor elements and bumps formed on the electrodes;

a space between ~~the~~ said first semiconductor elements and ~~the~~ said inner lead portions of ~~the~~ said lead frame is filled with an epoxy resin;

said two second semiconductor elements are stuck to surfaces opposite surfaces of ~~the~~ said first semiconductor elements stuck to ~~the~~ said lead frame by a semiconductor element adhesive;

one end of a wire is attached to an electrode disposed on a surface opposite the surface of each of ~~the~~ said second semiconductor elements stuck to each of ~~the~~ said first semiconductor elements;

the other end of the wire is attached to ~~the~~ a respective one of said middle inner lead portions of ~~the~~ said lead frame;

resin sealing is executed to include ~~the~~ said inner lead portions of ~~the~~ said lead frame and ~~the~~ said two pairs of first and second semiconductor elements; and

~~the~~ said outer lead portions of ~~the~~ said lead frame ~~is~~ are exposed from a resin-sealed portion.

5. (New) A semiconductor device comprising:

a lead frame having a plurality of arranged leads which each have an outer lead portion, a first inner lead portion and a second inner lead portion which is located between said first inner lead portion and said outer lead portion, said first inner lead portion having a first thickness and a first width, and said second inner lead portion having a second thickness which is larger than the first thickness and a second width which is larger than the first width;

a first semiconductor element mounted on said lead frame, said first semiconductor element having a surface and a plurality of first electrodes provided on said surface of said first semiconductor element, and each of said plurality of first electrodes of said first semiconductor element being respectively connected to said first inner lead portions of said plurality of leads by a bump;

a second semiconductor element mounted on said lead frame, said second semiconductor element having a surface and a plurality of second electrodes provided on said surface of said second semiconductor element, and each of said second electrodes of said second semiconductor element being respectively connected to said second inner lead portions of said plurality of leads by a wire.

6 (New) A semiconductor device according to the claim 5, wherein said lead frame has a first surface and a second surface which is opposite to the first surface, said first semiconductor element being mounted on said first surface of said lead frame, and said second semiconductor element being mounted on said second surface of said lead frame.

7 (New) A semiconductor device according to the claim 5, wherein said second semiconductor clement is formed on said first semiconductor element.

8 (New) A semiconductor device according to the claim 5, further comprising a resin sealing for sealing said lead frame, said first semiconductor element and said second semiconductor element.

9 (New) A semiconductor device according to the claim 8, wherein said outer lead portion of each of said plurality of leads is exposed from said resin sealing.